

High Temperature Superconductive Wideband Compressive Receivers

W. Gregory Lyons, *Member, IEEE*, Duane R. Arsenault, Alfredo C. Anderson, T. C. L. Gerhard Sollner, *Senior Member, IEEE*, Peter G. Murphy, Mark M. Seaver, Rene R. Boisvert, Richard L. Slattery, and Richard W. Ralston, *Senior Member, IEEE*

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Abstract—Wideband compressive receivers are an attractive application niche for analog high temperature superconductive (HTS) microwave filters. Chirp filters form the basis of compressive receivers, implementing a chirp-transform algorithm in the analog domain for real-time spectral analysis. HTS tapped-delay-line chirp filters are an enabling technology for instantaneous bandwidths greater than 1 GHz, and have evolved sufficiently to support dispersive delays as long as 40 ns with multigigahertz bandwidths and time-bandwidth products in excess of 100. Long dispersive delays have been obtained using a bonded/thinned-wafer technique to fabricate $\text{YBa}_2\text{Cu}_3\text{O}_{7-\delta}$ stripline devices on 5-mil-thick, 2-in-diameter LaAlO_3 substrates. These filters have produced better than -18 -dB error sidelobes. In addition, a 3-GHz-bandwidth HTS compressive cueing receiver was recently delivered to the Naval Research Laboratory to be flown on the high temperature superconductor space experiment (HTSSE), and demonstrations have been performed combining HTS chirp filters with conventional compressive-receiver hardware. A novel compressive cryoreceiver architecture is proposed combining HTS, cryoelectronic, and advanced high-speed semiconductor technologies. The proposed receiver will rival the sensitivity of a narrowband receiver while providing unprecedented wideband instantaneous frequency coverage. Future developments will extend the bandwidth capability. Detailed comparisons are made to an all-digital receiver and to channelized-filter receiver architectures. An HTS compressive receiver is projected to be clearly superior in overall size, weight, and power. Applications include electronic warfare and dynamic molecular spectroscopy for remote sensing.

I. INTRODUCTION

TREMENDOUS progress has been made since 1986 in the application of thin-film high temperature superconductors (HTS) to passive analog microwave filters [1]–[3]. High-quality HTS thin films with microwave surface resistances many orders of magnitude below that of copper at 77 K can now be reliably deposited over substrate areas as large as 3-in diameter. This has led to the implementation of a

large variety of HTS passive filter structures. Planar HTS devices offer a substantial size and weight advantage over low-loss waveguide structures, and the cryogenic operation affords the system engineer with the opportunity to achieve a very low noise receiver front-end. The planar nature of thin-film HTS devices allows the use of two-dimensional lithographic techniques to define filter structures rather than tedious and inaccurate three-dimensional machining techniques typically required for waveguides and dielectrics. Careful design of HTS microwave devices in conjunction with very low loss dielectrics at cryogenic temperatures may also allow higher Q s and lower losses to be obtained than is possible in conventional waveguide filters.

Passive microwave filters were an early favorite for HTS thin-film development efforts because of their simple, single-layer device structure. However, very low loss passive filters stress HTS film quality and design techniques as much as, for example, low-noise SQUID circuits. Roughly similar film quality is required for a low-loss or high- Q HTS microwave device with good power-handling capability as for a low-noise two-junction dc SQUID [4]. Now that good-quality HTS microwave devices can be made, research is focused on filter structures that will have the greatest system impact. The burden of cryogenic cooling must be justified by enabling a new level in system performance. The 4.2-K operation of conventional superconducting microwave devices has severely limited their application, despite the availability of closed-cycle 4-K refrigerators. The advent of HTS devices eases this cryogenic burden. Temperatures between 50–90 K enable the use of much simpler, smaller, more reliable, and less power-hungry cryogenic coolers, such as those in use or planned for infrared-imaging systems on remote-sensing satellites and military platforms [5].

Superconductive chirp filters represent an enabling technology because they support bandwidths beyond the 1-GHz limit of surface acoustic wave (SAW) compressive receiver technology [6] or the 2-GHz limit of acousto-optic channelizer technology [7], and because superconductivity is the only technology to successfully support multigigahertz bandwidths in an accurate chirp filter structure [8], [9]. The chirp filter and analog chirp-transform algorithm form the basis of a compressive receiver. This receiver performs spectral analysis in real time and with 100% time coverage, very attractive

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The authors are with the Analog Device Technology Group, Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, MA 02173-9108 USA.

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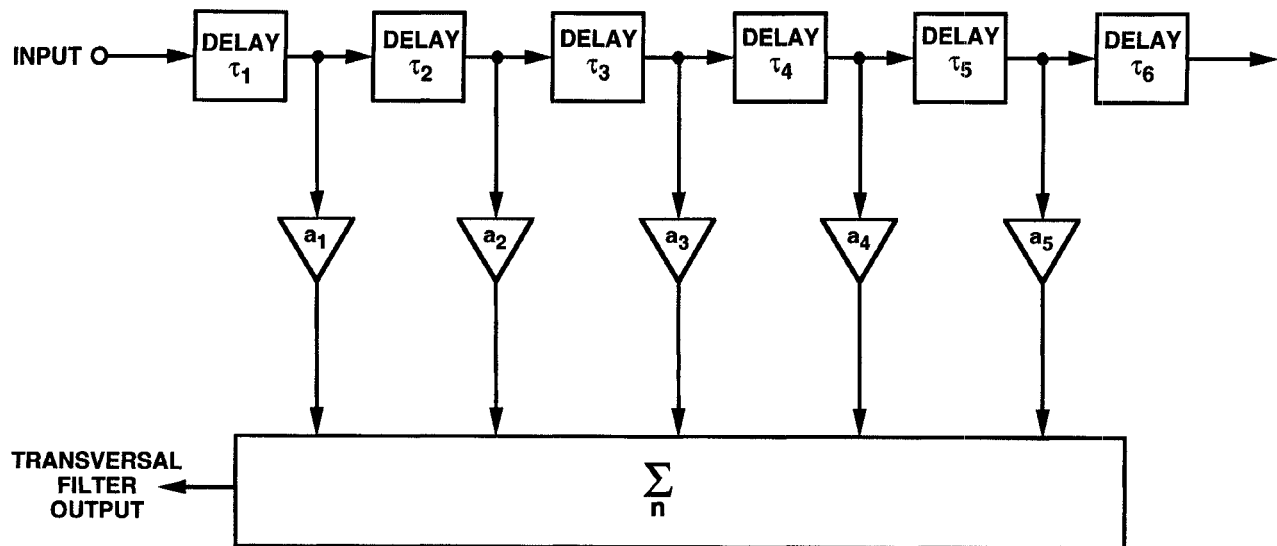


Fig. 1. Generalized transversal filter structure with time delays τ_i and tap weights a_i .

in military electronic warfare (EW) applications and dynamic molecular spectroscopy for remote sensing. These applications actually demand very wide bandwidth coverage, constantly pushing the state of the art in receivers. The size, weight, and power advantages of the HTS compressive receiver will be evident from comparisons made to an all-digital receiver and to channelized-filter architectures. Thus the application requirement exists today for HTS wideband compressive receivers, and chirp filters represent an attractive technology driver for HTS microwave devices.

II. SUPERCONDUCTIVE CHIRP FILTERS

A. Background and History

Chirp filters are the backbone of a compressive receiver and have also found extensive use in pulse-compression radars. Early work involved the use of folded tape meander lines, and crimped coaxial cable using reflections created by the impedance discontinuities at each crimp to provide the chirp filtering [8]. The acceptance of chirp filters as a system component did not really occur until large time-bandwidth-product, accurate SAW chirp filters were developed. But a wide variety of effects limit the bandwidth of SAW chirp filters, including propagation loss, transducer inefficiency, and difficulty in fabricating the submicron dimensions required by high-frequency transducers. Attempts have been made to build chirp devices using magnetostatic wave (MSW) media, but the tremendous dispersion in MSW materials makes this impractical [7]. For other chirp devices, such as crimped coaxial cable, loss and the device accuracy limit system applications.

The concept of a superconductive chirp filter was initially proposed by Lynch, and subsequently reduced to practice and patented [10], [11]. This work had grown out of an effort to build superconductive analog convolver structures in the GHz range, similar to ongoing research at the time into SAW-based devices [12]. The two advantages of supercon-

ductors in transmission-line structures are their extremely low loss at microwave frequencies and their nondispersive (i.e., frequency-independent) penetration depth. These advantages clearly lead to very long and compact electromagnetic delay lines. Introducing filter taps into these delay lines can produce a superconductive chirp filter that readily extends the bandwidth capability of chirp filters beyond the 1-GHz limitation of SAW devices.

An analog chirp filter is a form of a transversal filter. Fig. 1 outlines the generalized transversal filter structure. Filter taps provide samples of the input signal delayed in time by τ_i . These time-delayed samples are amplitude weighted by a_i and coherently summed to produce the filter output. Transversal filters are used to implement matched filtering, correlation, convolution, and Fourier transformation. The number of information cycles of the waveform gathered coherently in the filter determines the signal processing gain, measured conveniently as the time-bandwidth product.

An example of a fixed-tap-weight transversal filter is a linearly frequency-modulated delay line or chirp filter, also known as a dispersive delay line. Fig. 2 illustrates the operation of a proximity-tapped superconductive chirp filter [13], [14]. The transmission-line structure is typically stripline with upper and lower ground planes sandwiching the signal lines. This usually involves two substrates with signal lines and lower ground plane on opposite sides of the bottom substrate, and the upper ground plane on the top side of the top substrate. For clarity, only the signal lines are shown in Fig. 2. A series of backward-wave couplers achieves the downchirp (group delay increases as frequency decreases) filter response in direct analogy to a SAW chirp grating or transducer array. Each individual coupler has a peak response at the frequency for which it is a quarter-wavelength long. By making the reciprocal of the length of each coupler a linear function of the length along the line, the peak frequency response of the backward-wave couplers will vary as a linear function of delay. Weighting of the taps is achieved by varying the coupling strength between the two striplines forming each

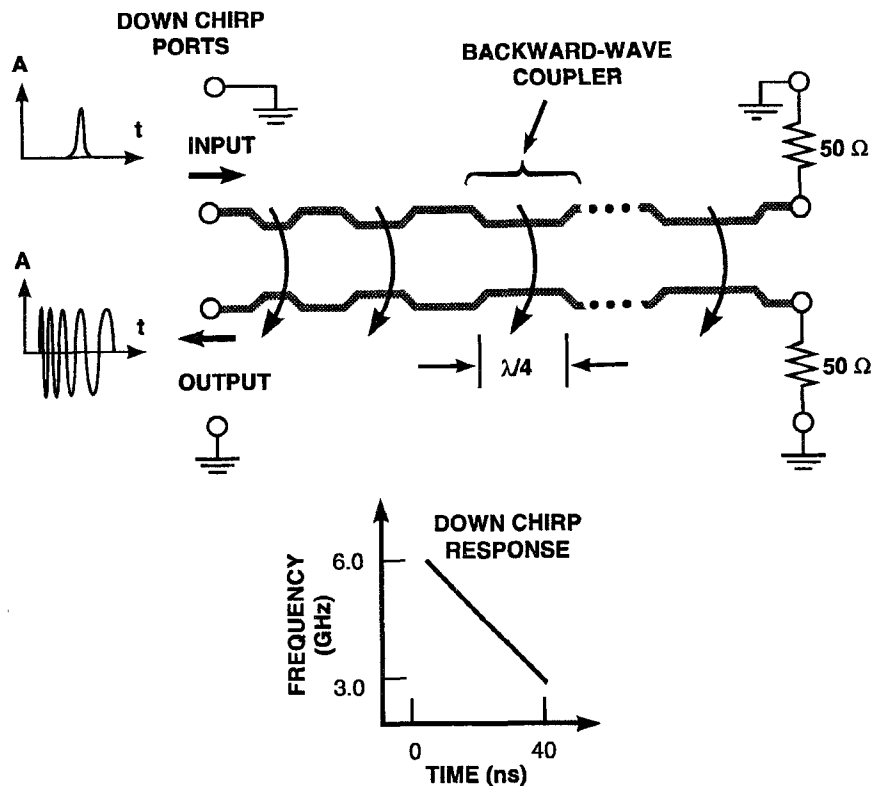


Fig. 2. Structure and operation of a proximity-tapped superconductive chirp filter. The downchirp impulse response is shown for a typical 3-GHz-bandwidth 40-ns-long chirp filter. The upchirp ports have been terminated into 50 Ω . The electromagnetic delay lines are implemented in stripline and the taps are implemented by a cascade of backward-wave couplers.

backward-wave coupler. Line-to-line isolation of greater than about -55 dB must be maintained in the uncoupled sections of the filter.

Fig. 2 diagrams the downchirp response of a superconductive chirp filter over a typical 3-GHz bandwidth with a dispersive delay of 40 ns. The device is symmetric and has both downchirp ports and upchirp ports. An impulse function applied to the downchirp ports will produce a downchirp signal over the bandwidth of the chirp filter, as shown. The 6.0-GHz component of the impulse couples to the output immediately while the 3.0-GHz component experiences the full delay of the filter.

Conversely an upchirp signal with the proper frequency-delay characteristic applied to the downchirp ports of the filter will be compressed into a pulse of width k/B_c and amplitude $(TB_c)^{1/2}$ above the input amplitude, where B_c is the chirp-filter bandwidth, T is the total dispersive delay, and k is a constant near unity determined by the filter weighting function. This pulse is referred to as a compressed pulse, and the action of the downchirp filter on the upchirp signal is matched filtering. As an example, Hamming weighting sets $k = 1.33$, giving a 0.44-ns mainlobe pulsewidth for $B_c = 3.0$ GHz. In addition to the k/B_c mainlobe pulsewidth, the compressed pulse has sidelobes whose ideal amplitude depends on the weighting function.

In direct analogy to a SAW grating or transducer array, the effective number of quarter-wavelength couplers N_{eff} active at a particular frequency f in a superconductive chirp filter

with dispersive delay T and bandwidth B_c is

$$N_{eff} = f \left(\frac{T}{B_c} \right)^{1/2}. \quad (1)$$

Thus, unlike the typical transversal filter, such as a CCD, where the time delay between the taps is constant and energy is tapped from a signal (for all relevant frequencies) across the full length of the device, the chirp filter effectively taps energy over only an N_{eff} grouping of couplers at a given frequency.

Several techniques can be used to design superconductive chirp filters. Initial work used the coupling-of-modes theory [15]. More recently, designs based on S - and T -matrix circuit analysis have been made possible by advances in the power of modern computers [16].

The material system of choice for the early work on superconductive chirp filters was niobium on high-resistivity silicon. After initial demonstrations of the concept and a demonstration of a chirp-transform algorithm [17], further work eventually yielded devices with error sidelobe levels of -32 dB, and bandwidths as large as 6 GHz [18]. An error sidelobe specification determines the allowable level of nonidealities in a chirp-filter response, which can be calculated using an analysis based on paired-echo theory [19]. In a compressed-pulse output, the error sidelobes rise up above the intentionally designed sidelobe levels obtained for a particular filter weighting function. For example, the ideal peak sidelobe level (with respect to the mainlobe) for Hamming weighting is -42.8 dB. An error sidelobe level of -32 dB corresponds to a

filter performance of 0.75-dB peak-to-peak amplitude accuracy and 5° peak-to-peak phase accuracy [20].

Reflectively tapped superconductive chirp filters were also designed and fabricated based on a well-defined impedance discontinuity at the tap points [15]. However, this structure is very susceptible to spurious reflections from defects and imperfections and has no input-to-output isolation, requiring a circulator for operation.

B. HTS Chirp Filters

The advent of high temperature superconductors has provided an opportunity to take the concept of superconductive chirp filters and move it into actual system application. Initial work focused on materials and processing issues, with some design consideration peculiar to the high-dielectric constant substrates. Historically, one of the first HTS devices demonstrated was an 8-ns 3-GHz-bandwidth $\text{YBa}_2\text{Cu}_3\text{O}_{7-\delta}$ (YBCO) chirp filter [21]. This was followed by the demonstration of a 12-ns 3-GHz-bandwidth YBCO chirp filter [22], [23] and finally a matched pair of 12-ns 3-GHz-bandwidth YBCO chirp filters, one flat weighted and the other Hamming weighted, used to generate a compressed pulse [24]. The matched filters exhibited -25 -dB error sidelobe performance, consistent with 2.2-dB peak-to-peak amplitude accuracy and 14° peak-to-peak phase accuracy [20]. This is competitive with very wideband SAW devices. This successful matched-filter demonstration enabled consideration of the HTSSE compressive cueing receiver described in Section IV.

Fig. 3 shows the measured electrical characteristics of one of these 12-ns Hamming-weighted filters, with a comparison between the designed and measured frequency-domain response. Chirp filters with the characteristics shown in Fig. 3 were also used later in the HTSSE prototype receiver. As shown in Fig. 3(a), the 5 dB of insertion loss is designed into the filter. This limits the strength of the backward-wave couplers enough to avoid distorting the input signal as it propagates through the tapped-delay-line chirp filter. Dissipation loss in this filter was unmeasurable. These first chirp filters were fabricated in a typical stripline configuration with YBCO signal lines and two silver ground planes on LaAlO_3 substrates. The 20-mil thickness of the brittle substrates limited the delay to 12 ns in order to avoid excessive line-to-line coupling in uncoupled sections. LaAlO_3 has become the substrate of choice for microwave applications because of its chemical, structural, and thermal-expansion match to YBCO, and its low microwave loss tangent (unusual for rare-earth perovskites).

There is an obvious discrepancy between the designed frequency response and the measured response shown in Fig. 3. One of the challenges presented by the LaAlO_3 substrate is the variation of the relative dielectric constant ϵ_r due to the crystallographic twins in the rhombohedral material. Measurements of narrowband filters [1] and the variation in the time-domain reflectometry response of a microstrip spiral line are consistent with an ϵ_r variation in LaAlO_3 of 1–2% [1], [23]. Lower frequencies will tend to average out the variation, while high frequencies and lumped-element circuits will see a larger variation. Other sources of degraded chirp filter performance

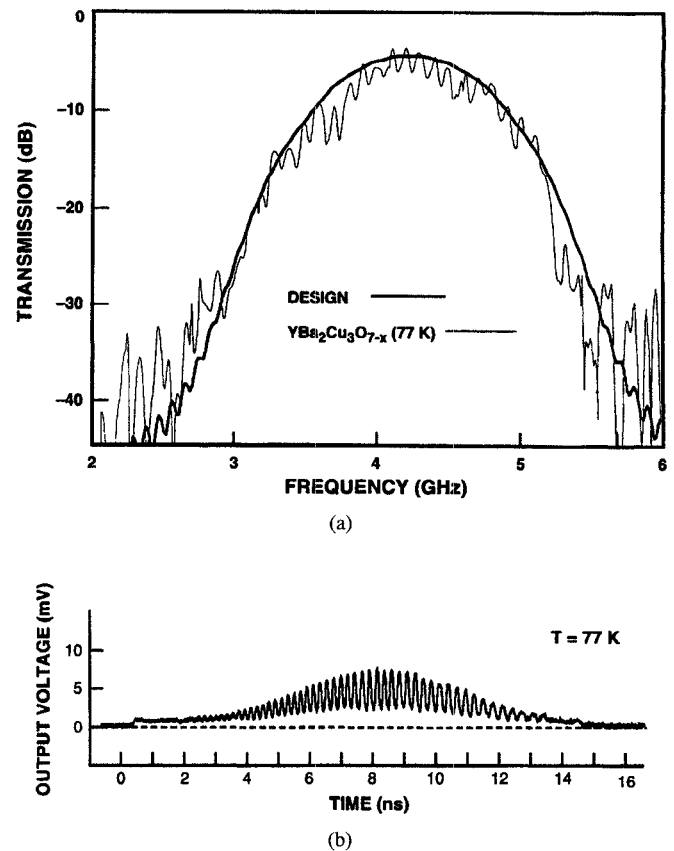


Fig. 3. (a) Frequency-domain response of a Hamming-weighted YBCO chirp filter at 77 K. The chirp filter has a bandwidth of 3 GHz, a center frequency of 4.2 GHz, a (designed) insertion loss of 5 dB, and a dispersive delay of 12 ns. (b) Downchirp time-domain response of a Hamming-weighted YBCO chirp filter at 77 K with the same parameters as in (a). The applied signal is a step function, and the response of each of the Hamming-weighted couplers can be discerned.

are YBCO film nonuniformities, nonuniformity in the wafer thickness, the microwave transition onto a high-dielectric constant material (ϵ_r is approximately 23.5 in LaAlO_3), air gaps in the stripline caused by surface undulations (more severe because of twinning), and packaging effects such as feedthrough. Feedthrough is clearly seen in the time-domain response of Fig. 3(b). Just past the 0-ns mark on the axis, prior to the response of the first coupler, the signal jumps up slightly as a result of input-port to output-port feedthrough. Another large source of error is forward coupling, and it is magnified by the length of the delay. This effect is absent in an ideal stripline, but in actual stripline devices, air gaps and ϵ_r variations degrade performance by causing the even- and odd-mode velocities to differ slightly. This mode velocity difference results in nonideal backward-wave couplers with a finite coupling coefficient in the forward direction.

Throughout this work, stripline was the preferred transmission media, just as it had been for niobium chirp filters. Microstrip is an unacceptable structure for proximity-tapped chirp filters because of the unequal even- and odd-mode velocities, which would result in tremendous forward coupling. Coplanar delay lines have the isolation and equal mode velocities required for backward-wave couplers, but require smaller dimensions than stripline to avoid moding problems and are

therefore more lossy than stripline. Some success has been achieved with coplanar waveguide for analog delay lines, but at the expense of inserting many air bridges to tie the two ground planes together [25]. Apparently the phase response of that coplanar structure is easily perturbed due to its similarity to a slow-wave filter, and as a result high-performance chirp filters would be difficult to realize in this manner.

HTS chirp filters have considerable advantages over filters made using conventional technology. For comparison, a 100-nm proximity-tapped chirp filter in room-temperature copper stripline would exhibit 75–100 dB of dissipation loss in the range 5–10 GHz [21], [26], [27], while an equivalent HTS chirp filter would produce negligible dissipation loss. Dispersion due to the frequency-dependent skin depth in the normal metal would also be a tremendous problem, as would the very thick metal layer required to achieve even that level of loss. Compared to SAW chirp filters which often require ovens to generate a thermally stable environment, the HTS filters are already in a temperature-controlled cryogenic environment. When operated below approximately 60 K, YBCO HTS filters have little temperature dependence because the superconducting properties (order parameter and superconductor gap) change very little at two-thirds of the transition temperature. SAW devices also produce at least 20 dB more insertion loss than HTS filters. Furthermore, due to the slow propagation velocity of SAW's, devices are very difficult to build accurately at high frequencies where the structural dimensions become exceedingly small. Typical SAW wavelengths are on the order of 5–10 μm . Submicron lithography control must be applied to the transducer structures. The situation is very different for HTS chirp filters because they are based on electromagnetic delay lines with wavelengths on the order of many millimeters. This larger wavelength relaxes the dimensional control requirement somewhat, but lengths in the third dimension such as substrate thickness do become an issue.

III. CONCEPT OF COMPRESSIVE RECEIVER

A. Chirp-Transform Algorithm

The concept of a compressive receiver and chirp filters dates back to at least White's patent on the compressive receiver [28]. The chirp-transform algorithm [8], [29]–[34] which is the basis of the compressive receiver can be understood by starting with a standard Fourier transform

$$H(\omega) = \int_{-\infty}^{\infty} h(\tau) \exp(-i\omega\tau) d\tau \quad (2)$$

and performing a linear mapping of frequency into time by $\omega = \mu t$ with μ the chirp slope (rate of linear frequency change with time). This can be written as

$$-i\omega\tau = \frac{i\mu(t - \tau)^2}{2} - \frac{i\mu t^2}{2} - \frac{i\mu\tau^2}{2} \quad (3)$$

and the expression for the Fourier transform becomes a chirp transform

$$H(\mu t) = \exp\left(\frac{-i\mu t^2}{2}\right) \int_{-\infty}^{\infty} \left[h(\tau) \exp\left(\frac{-i\mu\tau^2}{2}\right) \right]$$

$$\cdot \exp\left[\frac{i\mu(t - \tau)^2}{2}\right] d\tau \quad (4)$$

using infinitely long chirp signals in the same way the Fourier transform makes use of infinitely long sinusoids. The expression inside the square brackets represents a Multiplication of the signal $h(t)$ with a chirp signal. A Convolution with a chirp of opposite slope is performed by the integration. Finally, another Multiplication is done with a chirp signal of the same chirp slope as the first multiplication. This is known as an MCM chirp transform and produces the complete Fourier transform of the input signal, where frequency, amplitude and absolute phase are all mapped into time. Taking the Fourier transform of (4), and recalling that convolution in one domain becomes multiplication in the other and that chirps transform to chirps demonstrates that a CMC configuration will implement the same chirp transform. These continuous chirp transforms are not to be confused with a chirp-Z transform, which is a sampled version of this analog chirp transform and is implemented digitally or with CCD's [30]. In actual microwave implementations, multiplication with a chirp is performed using a chirped local oscillator and a mixer. Convolution with a chirp is realized by passing the signal through a chirp filter.

The finite length of actual chirp signals and filters leads to two possible, implementable *full* chirp transforms, the M(s)–C(l)–M(s) and the C(s)–M(l)–C(s), where l stands for long and s means short. Typically the long chirp is twice the length and bandwidth of the short chirp. If only frequency, amplitude, and relative phase between two channels is important, the final M of the MCM or the first C of the CMC can be dropped. Absolute phase information requires a full MCM or CMC. This leaves two possible algorithms for a compressive receiver, M(l)–C(s) and M(s)–C(l). There are advantages to each [35]. The M(l)–C(s) system is most often used, but requires alternating between a pair of channels to achieve 100% time coverage. The M(s)–C(l) system requires only a single channel, but effectively halves the length of the filter for the convolution [C(l) must be twice the size of C(s) for the same frequency coverage] and a single-channel implementation has difficulty with out-of-band signals and filter triple-transit effects. An additional feature of the M(l)–C(s) system is the ability to readily increase the frequency coverage by lengthening the multiplying chirp to overscan the bandwidth of the convolving chirp filter while maintaining the same chirp slope. This extends the bandwidth coverage of the receiver at the expense of reduced time coverage. The M(l)–C(s) is often referred to as a microscan or sliding-transform receiver.

Fig. 4 illustrates the operation of an M(l)–C(s) receiver. Input signals over the receiver bandwidth B_R are multiplied with a chirp signal of length $2T$ and bandwidth $2B_c$, with T the dispersive delay and B_c the bandwidth of the chirp filter, respectively. The multiplication (mixing) process produces a set of frequency-offset chirp signals, where each offset is determined by the input frequency. This set of chirp signals is convolved by the chirp filter, producing a compressed pulse at the output of the filter for each input signal. The exit time

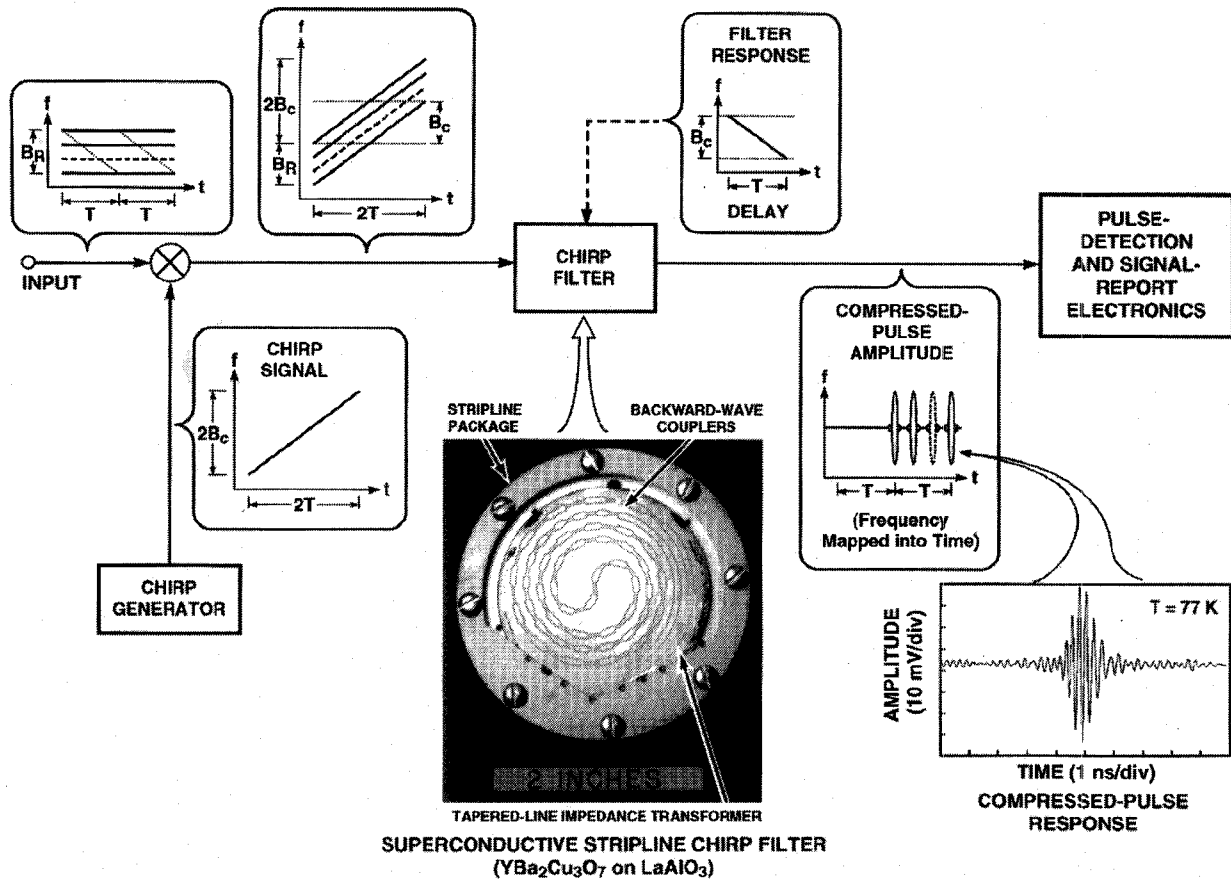


Fig. 4. System diagram of a compressive receiver M(l)-C(s) chirp-transform algorithm with receiver bandwidth B_R , chirp filter bandwidth B_c , and chirp filter dispersive delay T . This architecture is well suited to extract the frequency and amplitude of input signals. The measured 77-K compressed pulse response of a matched pair of YBCO chirp filters and a photograph of a 12-ns YBCO chirp filter are shown as insets.

and amplitude of these compressed pulses are directly related to the input signal frequency and amplitude. The chirp filter must have the same chirp-slope magnitude but opposite sign relative to the chirp-signal generator. As indicated in Fig. 4, mixing input signals over a bandwidth B_R with a swept local oscillator (SLO) of bandwidth $2B_c$ generates chirp signals that cover a frequency range $B_R + 2B_c$. Only B_c of that range is within the bandwidth of the chirp filter so that a compressed pulse will be produced. This causes the input analysis window to actually be frequency dependent or slide in time, as shown in Fig. 4. Overscan simply extends the SLO sweep to cover more bandwidth, and percent time coverage is inversely proportional to the overscan ratio. Referring to Fig. 4, and assuming two alternating M(l)-C(s) channels for 100% time coverage of receiver bandwidth B_R with SLO scan over B_S

$$\begin{aligned} \text{Overscan ratio} &= \frac{(B_S - 2B_c) + B_c}{B_c} \\ &= \frac{B_S - B_c}{B_c} \end{aligned} \quad (5)$$

$$\text{Time coverage} = \frac{1}{\text{overscan ratio}}. \quad (6)$$

For example, to cover 10 GHz with a 3-GHz chirp filter requires an SLO scan of 13 GHz for a 3.3 overscan ratio and 30% time coverage.

Fig. 4 highlights the fact that the enabling device technology for a 3-GHz-bandwidth chirp transform is the HTS chirp filter. Conventional technology can be used to build the other components quite adequately, as will be seen in the following sections.

Table I lists the frequency resolution $\Delta f = k/T$ of an M(l)-C(s) compressive receiver [6] using Hamming-weighted chirp filters, for which $k = 1.33$ [36] and where T is the total dispersive delay of the filter. The range of delays shown is consistent with present HTS chirp-filter capabilities as described later in this paper. The -3-dB pulsewidth is used as a criterion for resolution. The compressed-pulse mainlobe width is still k/B_c , as for the matched filter example in Section II. The frequency resolution Δf is determined by dividing the bandwidth B_c by the number of k/B_c pulsewidths that fit into an analysis window of length T , or $\Delta f = B_c/[T/(k/B_c)] = k/T$ and is independent of B_c . Table II translates the -3-dB pulsewidth of the compressed-pulse envelope into a logic speed required to capture samples separated in time by this pulsewidth. This logic speed produces a 3.0-dB accuracy in determining compressed pulse amplitudes.

B. Comparison of Receivers

There exists a wide variety of receivers that have been used in electronic warfare applications. The most common can be classified as superheterodyne, compressive, channelized-filter,

TABLE I
FREQUENCY RESOLUTION AS A FUNCTION OF HAMMING-WEIGHTED CHIRP-FILTER DISPERSIVE DELAY FOR AN M(l)-C(s) COMPRESSIVE RECEIVER

Dispersive Delay (ns)	Frequency Resolution (MHz)	"Bins" per GHz
8	166	6.0
12	111	9.0
24	55.4	18.0
40	33.3	30.1
100	13.3	75.2
200	6.7	150.4

TABLE II
PULSEWIDTH (−3 dB) OF HAMMING-WEIGHTED COMPRESSED-PULSE ENVELOPE
AND PULSE-DETECTION LOGIC SPEED FOR 3.0-dB AMPLITUDE ACCURACY

Chirp Filter Bandwidth (GHz)	Compressed-Pulse Width (ns)	Pulse-Detection Logic Speed (GS/s)
2.0	0.67	1.5
2.5	0.53	1.9
3.0	0.44	2.3
4.0	0.33	3.0
5.0	0.27	3.8
10.0	0.13	7.5

acousto-optic channelized, instantaneous frequency measurement (IFM), and crystal video receivers [8], [29]. Future receivers need to perform well in dense signal environments over many tens of GHz. The key requirement for future receivers is excellent wideband simultaneous-signal performance and 100% time coverage.

These considerations can very quickly limit future advanced EW receiver choices to compressive receivers and channelized receivers. Crystal video and IFM receivers do not function well in the presence of more than a single emitter. Superheterodyne receivers have a poor probability of intercept (time coverage) because of their narrowband nature [8], despite their excellent dynamic range, sensitivity, and resolution. A superheterodyne IF filter with a bandwidth B will have a response time of $1/B$. The fastest superheterodyne scan rate without degrading sensitivity is approximately $B/(1/B) = B^2$. For example, if the IF filter bandwidth is 10 MHz, then the fastest scan rate is 100 MHz/ μ s. If the input bandwidth is 10 GHz, then the superheterodyne receiver will take at least 100 μ s to scan across the entire band. Obviously, there is a finite probability that any pulses shorter than 100 μ s will be missed by the receiver. In this example, at any one time the superheterodyne receiver is looking at 10 MHz/10 GHz = 0.1% of the input bandwidth.

Channelized-filter receivers will be considered in more detail in Section VIII as part of a direct comparison to an HTS compressive receiver. A major issue for channelized-filter architectures is the very large number of individual filters required. On the other hand, acousto-optic channelized receivers [7] achieve channelization in a very compact Bragg cell [37]. This is a very efficient architecture, particularly for frequency activity indication. However, acousto-optic receivers do have some potential weaknesses. The full parameterization

of emitters is often slow because of the parallel nature of the receiver output and the need to quickly sample these outputs. This has forced the use of very high speed analog multiplexing circuits to serialize the channelizer output to a speed compatible with processing on a monolithic chip and at a frame rate fast enough to determine timing details (such as pulse width) of the intercepted emitters. The most mature acousto-optic technology (power spectrum channelizer) does not allow relative phase information to be extracted, although acousto-optic heterodyne techniques are rapidly improving. Finally, the bulk acoustic technology is limited to 2-GHz analysis bandwidths.

The significant challenge facing compressive receivers is the required high-speed output circuitry due to the serial nature of the receiver output. As noted for acousto-optic receivers, data in a serial form has significant advantages if available circuits can achieve the required speed. Semiconductor technology is beginning to produce circuits well matched to the multigigahertz bandwidths of HTS compressive receivers. In Section VII we describe an architecture utilizing some of these circuits.

IV. HTSSE II COMPRESSIVE CUEING RECEIVER

A. HTSSE Cueing Receiver Concept and Hardware

A cueing receiver is a spectrum activity indicator, producing frequency information on emitters that can be used to cue additional receiver assets onto active signals of interest [8]. Representing an example of a promising HTS subsystem, Lincoln Laboratory delivered both flight and qualification versions of an HTS wideband compressive cueing receiver to the Naval Research Laboratory (NRL) for the Navy's second high temperature superconductor space experiment (HTSSE II) [38], [39]. This followed the production of a breadboard version of the receiver [40] and the delivery to NRL of a prototype [41]. The simplest form of a compressive receiver was chosen for these demonstrations. The system combines an HTS chirp-transform subsystem with high-speed semiconductor compressed-pulse processing circuits.

Fig. 5 illustrates the operation of this receiver with a block diagram. An M(l)-C(s) chirp-transform algorithm is utilized with a 3.0-GHz-bandwidth YBCO chirp filter and a chirp generator consisting of a fast voltage-ramp generator driving a voltage-controlled oscillator (VCO) to produce a flat-weighted chirp signal. The compressed-pulse-detection portion of the system latches the value of a 2-GHz digital counter whenever

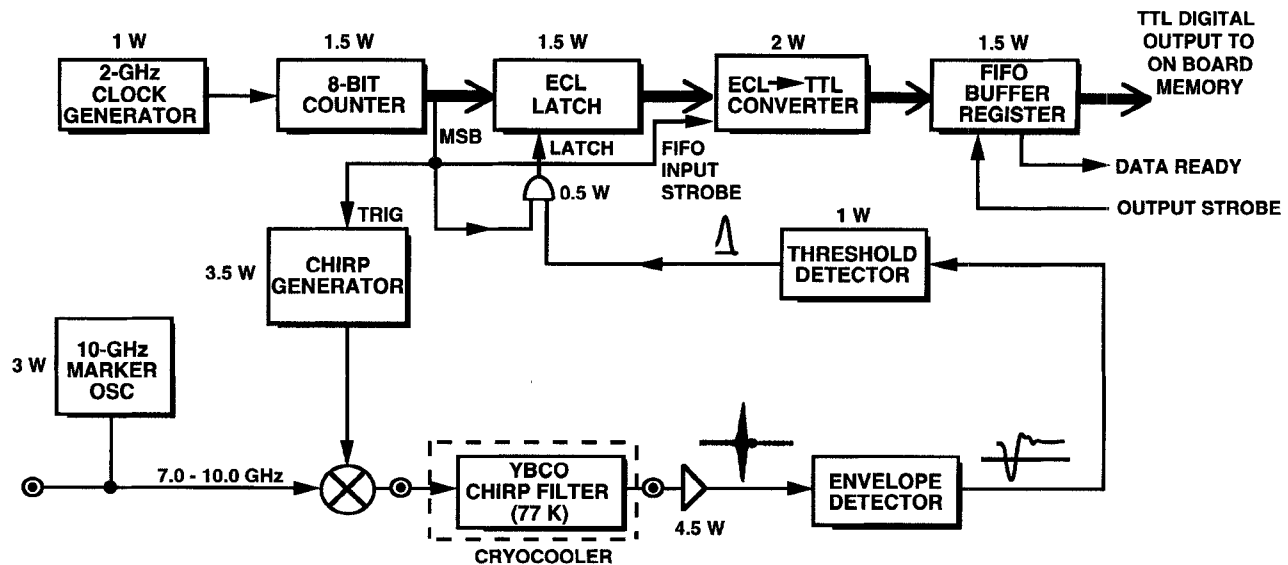


Fig. 5. System block diagram of the HTSSE II compressive cueing receiver. Signal waveforms are shown as insets. The space-qualified version of the receiver covered 7.0–10.0 GHz, while the prototype covered 9.4–12.4 GHz. A 10-GHz oscillator was added to the input of the space-qualified receiver as an end-of-band marker. The power consumption quoted on the figure was measured on the space-qualified receiver.

a compressed pulse above a fixed threshold is detected coming out of the chirp-transform subsystem. This records the time a compressed pulse exits the chirp-transform subsystem and therefore records the frequency of the detected input signal via a look-up table. A 2-GHz oscillator serves as the clock generator that drives an 8-bit silicon ECL ripple counter. The counter runs continuously. The most significant bit (MSB) is used as a reset trigger (TRIG) to the chirp generator, thereby setting the chirp-transform analysis window equal to $2^8(0.5 \text{ ns}) = 128 \text{ ns}$. Valid data is accepted only while the MSB is high. The 2-GHz counter rate is required because a frequency bin corresponds to the -3-dB pulsewidth of a 3-GHz-bandwidth Hamming-weighted compressed pulse, approximately 0.5 ns, as seen in Table II.

A compressed pulse generated by a signal at the input to the receiver is passed through an envelope detector to remove the carrier frequency. This compressed-pulse envelope (negative portion of envelope) is then passed through a threshold detector (acting as an inverter) that strobes a silicon ECL logic gate to produce an appropriate logic level to latch the 8-bit counter value into an 8-bit ECL latch. The output of the counter is passed on to a first-in first-out (FIFO) buffer register following a voltage level conversion from ECL to TTL. The FIFO contents are then available to the satellite data bus and memory.

A 10-GHz oscillator was included on the qualification and flight versions of the receiver to produce an end-of-band marker for on-orbit receiver calibration. The power consumption of the various room-temperature components is also indicated in Fig. 5. The semiconductor ECL components are clearly very costly to the power budget. The amplifier following the chirp filter is required to overcome the insertion loss of the mixer, cryogenic cables, and chirp filter, and then drive the envelope detector at a sufficient signal level to ensure linear performance from the detector. The compressed pulse, envelope-detected compressed pulse, and logic compatible

pulse waveforms are all shown as insets in Fig. 5. Fig. 6 shows a typical compressed pulse and compressed-pulse envelope produced by all (breadboard, prototype, qualification, and flight) versions of the receiver.

Projections for the available power on board the satellite forced the Navy to limit the cueing receiver power budget to 20 W. Therefore, only the single ECL latch shown in Fig. 5 could be included, limiting the receiver to determining the frequency of only one test signal within the 3-GHz instantaneous analysis bandwidth. Multiple-signal capture has previously been demonstrated for this receiver configuration [40], but would have required a 4-W power increase per additional signal detection. As configured, the cueing receiver detects the 10-GHz oscillator signal (for end-of-band calibration) unless a test signal within the band of the receiver is being sent to the satellite from the ground. The test signal would then be detected in the presence of the 10-GHz marker signal, demonstrating the capability of the receiver configuration to detect multiple simultaneous signals.

Fig. 7 is a photograph of the prototype HTSSE compressive cueing receiver. The measured electrical responses of the YBCO chirp filter used in the prototype receiver were shown in Fig. 3. Fig. 8(a) shows the space-qualified 12-ns YBCO chirp filter. Fig. 8(b) shows the space-qualified ambient-temperature electronics portions of the receiver. The addition of the 10-GHz oscillator and a shift in the chirp-filter center frequency from 4.2 to 6.7 GHz (to accommodate a 7.0–10.0-GHz input band) were the only significant differences between the prototype and flight versions.

B. Fabrication and Space-Qualification of Hardware

The cryogenic YBCO chirp filter shown in Fig. 8(a) is a stripline configuration, with an upper and a lower 2-in-diameter LaAlO_3 substrate squeezed together by an array of springs [24]. The upper substrate supports a single silver ground plane, while the lower substrate has the patterned

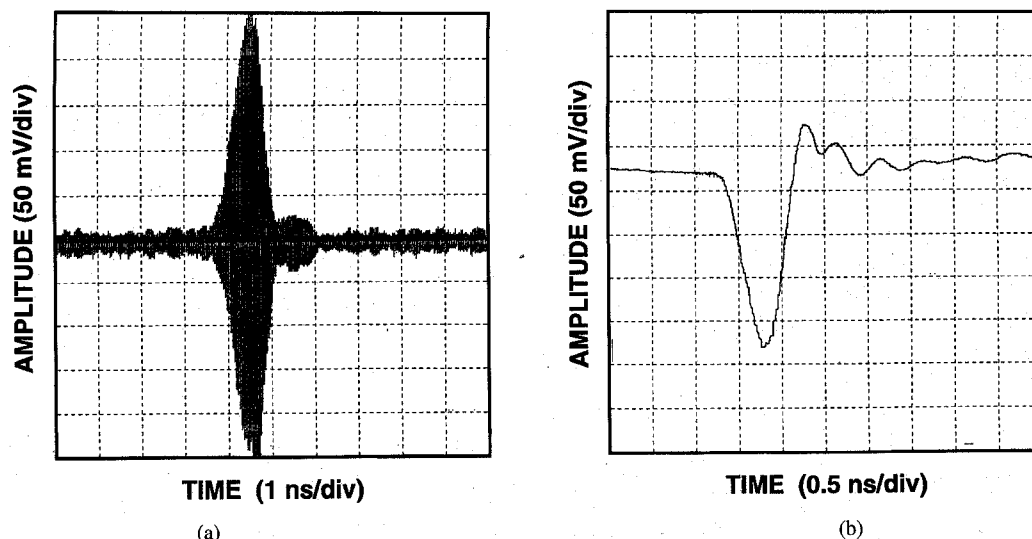


Fig. 6. (a) Typical compressed-pulse output from the YBCO chirp filter in HTSSE compressive cueing receiver. (b) Typical compressed-pulse envelope in HTSSE compressive cueing receiver.

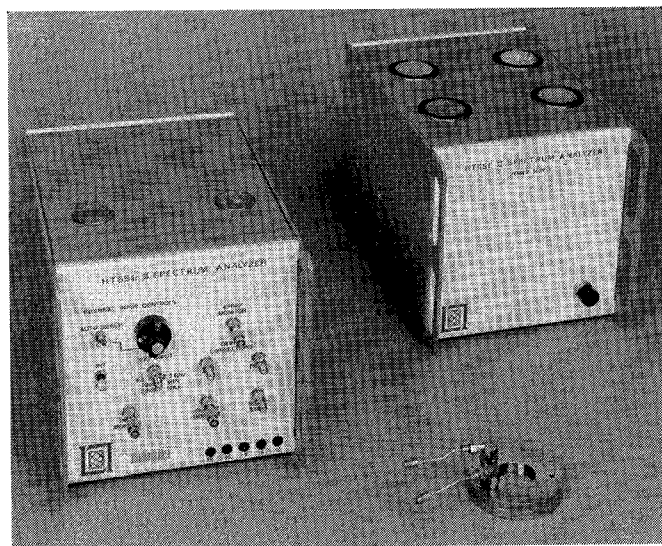


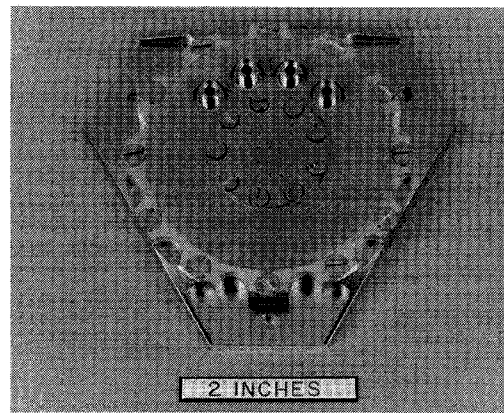
Fig. 7. Prototype HTSSE compressive cueing receiver. The HTS chirp filter, room-temperature electronics box, and power supply box are shown. The height, width, and depth of both of the electronics boxes are 7, 7, and 9 in, respectively.

YBCO tapped-delay-line chirp filter on one side and a silver ground plane on the other. The 165 BeCu springs hold the two substrates against an aluminum base plated with 125 μin of 24-K gold. The spring force is sufficient to generate enough static friction to prevent the substrates from moving under the specified mechanical stress. The base of the cryogenic filter package is clamped to the Navy's cryogenic bus using spring loaded bolts and an indium gasket. The cryogenic package was hermetically sealed to prevent degradation of the YBCO which can occur when YBCO comes in contact with moisture and CO_2 . The hermetic seal was implemented by sealing the package in a pressurized neon gas atmosphere using indium wire gaskets. The indium wire gasket technique used was similar to a procedure extensively investigated for use with SAW devices on the Navy FLTSAT FEP satellite program [42] and the joint Lincoln/COMSAT/AT&T delivery

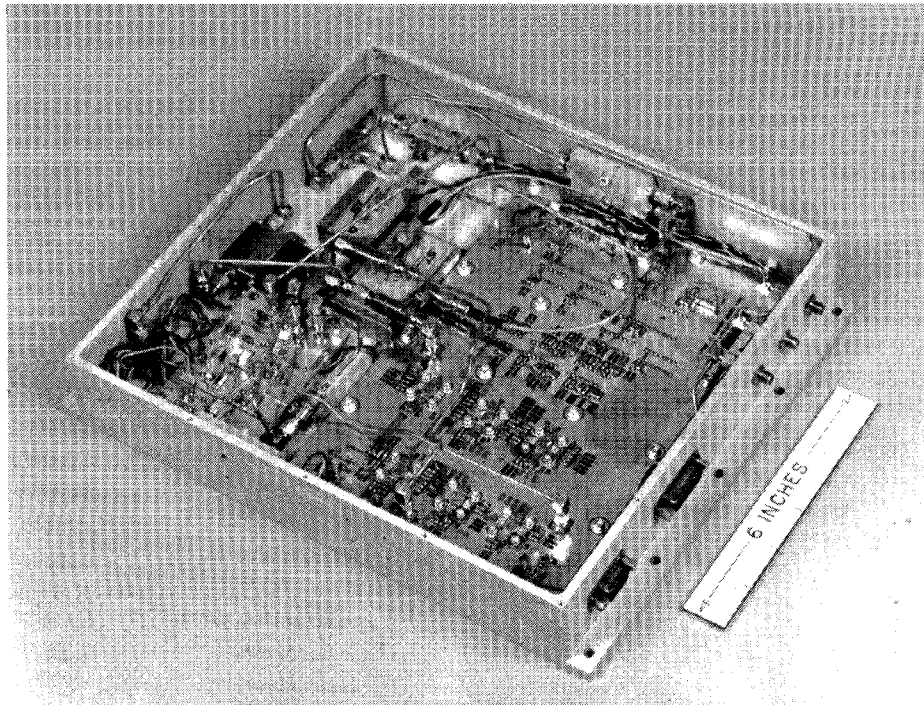
of a narrowband YBCO filter for HTSSE I [43]. The cryogenic package was leak checked with a residual gas analyzer to establish a leak rate of less than 4×10^{-9} Torr-liter/s. The package has a base footprint of 7 sq in. Total package height is approximately 0.5 in, with an aluminum package base that is 0.13 in thick.

The fabrication of the YBCO chirp filter followed most of the standard procedures initiated prior to HTSSE I [1], [43]. A 4- μm layer of silver preceded by a 200- \AA layer of titanium was used for both upper and lower ground planes. Patterning of the YBCO signal lines was accomplished with standard photoresist and a spray-etch of 0.25% H_2PO_4 , which successfully prevents the residual film formation typically seen with other wet-etching methods. Undercutting on the order of 1 μm is observed with this etch. Several techniques have been used for ohmic contact formation. The most successful has been a standard photoresist procedure with an *in-situ* ion-beam etch followed by e-beam evaporation of 1.5 μm of Ag. Following photoresist lift-off, the contacts are annealed in flowing O_2 for 1 h followed by a slow ramp to room temperature. Final packaging for the space-qualified HTSSE II devices was performed using ultrasonic wedge bonding of 0.5 \times 3-mil Au ribbon directly on the annealed Ag contacts. These procedures yielded low contact resistances and good bond-pull strengths. The electrical responses of the space-qualified versions of the chirp filters were very similar to that shown in Fig. 3, with a shift in center frequency to 6.7 GHz. The HTSSE devices utilized off-axis sputtered YBCO thin films [44] with typical best parameters of $T_c = 88$ K, J_c (77 K) > 2 MA/cm², and R^S (77 K, 10 GHz) = 500 $\mu\Omega/\text{sq}$. The 12-ns length did not require values quite this low to achieve negligible dissipation loss. More recent work with longer delays has used films grown by a cylindrical magnetron, achieving these excellent parameters as standard performance [45].

Extensive work was performed to ensure that the ambient-temperature electronics box and the cryogenic YBCO chirp filter would survive an orbital rocket launch and the subsequent space environment. After a qualification version of both the



(a)



(b)

Fig. 8. (a) Space-qualified cryogenic package for the final HTSSE compressive cueing receiver. This hermetically sealed package contains the 12-ns YBCO chirp filter in a stripline configuration. (b) Space-qualified package containing the ambient-temperature pulse detection and frequency-report electronics, mixer, and chirp generator portions of the final HTSSE compressive cueing receiver.

ambient box and chirp filter were fabricated and tested, final flight versions were fabricated with any necessary modifications. Details on the space-qualification procedure can be found in [39].

C. Final Space-Qualified HTSSE Cueing Receiver Performance

A plot of frequency-report-bin number versus input-signal frequency is shown in Fig. 9 for the space-qualified flight receiver. The number of frequency bins is determined by the width of the compressed pulses and the length of the chirp filter. The 3-GHz bandwidth and Hamming weighting of the chirp filter produce a compressed pulse that is 0.44 ns wide. The dispersive length of the chirp filter is 12 ns. Therefore, the analysis window of the compressive receiver will support 28

frequency bins, providing the 110-MHz frequency resolution. Timing jitter on the order of 30 ps limited the definition of the width of a bin to approximately 10 MHz.

The chirp generator deviates from a linear frequency-versus-time slope significantly more than the chirp filter [40], and thereby sets an error sidelobe level of 19 dB. These error sidelobes act just as spurious signals would in a compressive receiver, limiting the dynamic range of the system to 19 dB because of the single fixed threshold crossing used for compressed-pulse detection. A multiple-threshold receiver using the same technology could support a single-signal dynamic range of 60 dB and a two-signal dynamic range of at least 19 dB. The amplitude of the envelope-detected compressed pulse deviates by less than 3 dB across the 3-GHz analysis bandwidth.

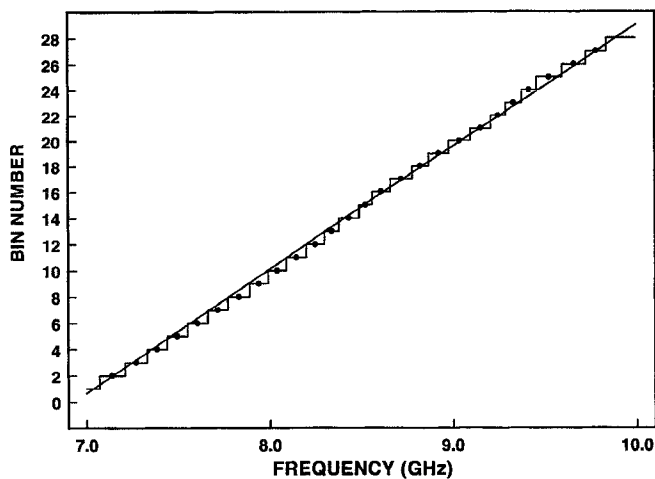


Fig. 9. Frequency-report-bin number versus input-signal frequency for the final flight version of the HTSSE compressive cueing receiver. The frequency midpoint of each frequency-report bin is indicated. The straight line shows the ideal location of each midpoint, which would correspond to uniform-width frequency bins. The average bin width is 110.0 MHz. This is equal to the ideal bin width for 12-ns chirp filters. The maximum deviation from this ideal width is 30 MHz, and 40% of the bin widths are equal to 110 MHz.

However, this 3-dB pulse amplitude variation, which can be traced directly to nonlinearities in the SLO, has a significant effect on the width of each frequency-report bin. An increase in pulse amplitude causes the pulse to be detected sooner than ideal, and a decrease delays the detection. Fig. 9 indicates the frequency midpoint of each bin and the straight line illustrates the ideal location of each midpoint. Increases in pulse amplitude push the midpoint above the line and shorten the bin widths. Decreases in pulse amplitude have the opposite effect. The movement of the midpoint with respect to the line (and the bin widths) very closely tracks the measured compressed-pulse amplitude variation across the band, and can account for the maximum deviation of 30 MHz from the ideal bin width of 110 MHz.

The operating characteristics for the space-qualified compressive cueing receiver are summarized in Table III. The analysis bandwidth, frequency resolution, and number of frequency bins are readily evident from Fig. 9. The 128-ns analysis time was limited by the speed with which the chirp generator can reset itself and begin a new frequency sweep. Above 83 K the YBCO chirp filter is too close to the superconducting transition temperature to function properly. The ambient power consumption of 20 W is clearly dominated by the discrete high-speed semiconductor ECL logic operating at 2 GHz. A future version of this receiver would make use of rapidly emerging, commercially available, monolithic high-speed components that provide far greater digital processing capability with far less power consumption per gate.

V. BONDED/THINNED-WAFER HTS CHIRP FILTERS

As indicated in Table I the frequency resolution of a compressive receiver is tied directly to the dispersive delay of the chirp filters. The HTS chirp filters are based on a stripline configuration that uses two symmetrically placed ground planes on opposite sides of a pair of wafers. As a result,

the packing density of the delay lines and therefore the total chirp filter length is inversely proportional to the thickness of the two wafers. Standard 20-mil-thick, 2-in-diameter LaAlO_3 wafers limit the delay, with appropriate line-to-line isolation, to approximately 12 ns as used in the HTSSE compressive cueing receiver. A bonded/thinned-wafer technique has been developed to increase the delay achieved on a 2-in-diameter LaAlO_3 wafer to first 24 ns [46] and then to 40 ns [47]. This is a refinement of a technique used to demonstrate 44-ns YBCO analog delay lines [27]. As the wafer thickness is reduced to 10 mil and less to allow more delay, a support wafer is required to prevent the thin wafer from breaking. Fig. 10 diagrams the technique used to bond and thin a 2-in-diameter LaAlO_3 wafer, and shows a photograph of a 40-ns YBCO chirp filter fabricated using the technique.

The wafer-bonding process begins with a 20-mil-thick LaAlO_3 upper wafer with a sputtered layer of Ti/Au (300 Å of Ti followed by 2 μm of Au) on the bottom surface, a 20-mil-thick LaAlO_3 base wafer with a sputtered layer of Ti/Au on the top surface, and a 10- μm -thick gold foil. The two wafers and the gold foil must be kept very clean throughout the entire process. The wafers are forced together against the gold foil in a hot press inside an oxygen atmosphere.

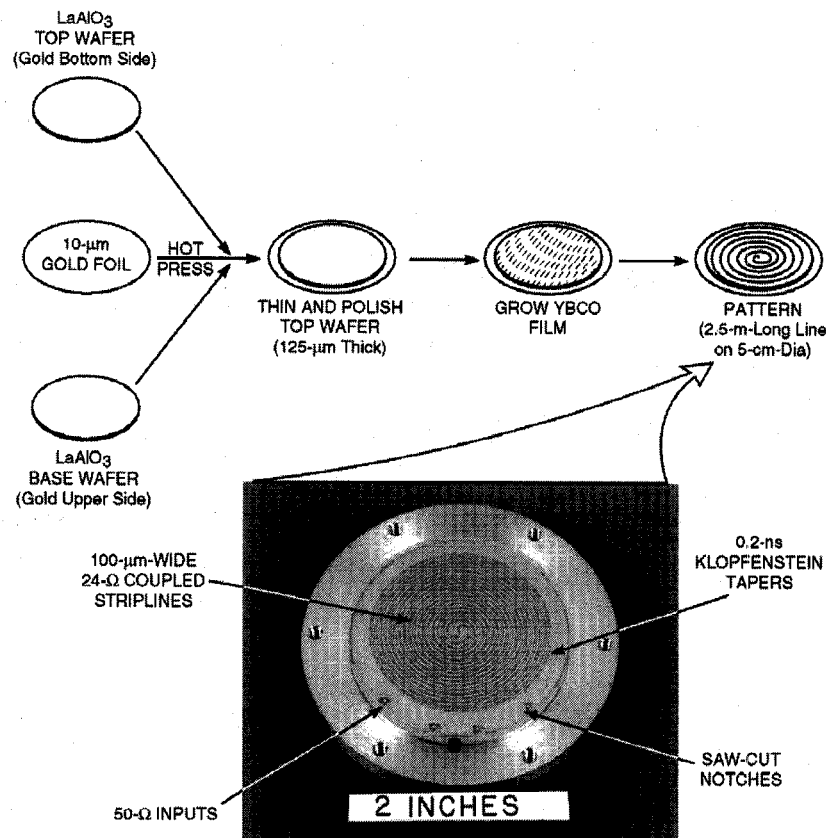
The top wafer is lapped to a thickness of 190 μm , and then polished using chemical-mechanical polishing compound to a final thickness of 125 μm . The polished surface must be compatible with epitaxial growth of YBCO. After polishing, the bonded-wafer pair is placed in a standard gas pocket heater, and growth of YBCO is performed with a cylindrical magnetron on the top surface of the thin wafer [45]. Standard YBCO patterning techniques can be used following the YBCO growth. A layer of gold, electroplated onto the sides of the wafer, contacts the edges of the gold foil to complete the contact to the ground plane on the bottom surface of the thin wafer. A second bonded-wafer pair is required for the upper ground plane of the stripline configuration.

The initial demonstration of 24-ns YBCO chirp filters was done by bonding existing 10-mil-thick LaAlO_3 wafers to a 20-mil-thick LaAlO_3 carrier wafer and skipping the wafer thinning step shown in Fig. 10. The initial demonstration of the 40-ns YBCO chirp filters on 5-mil-thick LaAlO_3 used the entire procedure indicated in Fig. 10. The 24-ns YBCO chirp filters in combination with a modified HTSSE VCO-based SLO produced error sidelobes better than -18 dB, limited by the performance of the SLO [40]. The experimental test configuration is shown in Fig. 11(a), essentially a M(l)-C(s) receiver front end. The 24-ns filter consists of 96 backward-wave couplers, implemented in 100- μm -wide 32- Ω stripline. However, the initial 40-ns YBCO chirp filters produced error sidelobes of only -13 dB with a similar SLO [47]. The longer dispersive delay clearly made the device more susceptible to device imperfections such as forward coupling and poor microwave transitions. The 40-ns filters consist of 160 backward-wave couplers, implemented in 100- μm -wide 24- Ω stripline.

Improvements have been made to the 40-ns chirp filter by saw cutting notches in the edge of the wafer and gold plating the inside of the notches. This is done to reduce reflections at

TABLE III
OPERATING CHARACTERISTICS OF FINAL SPACE-QUALIFIED HTSSE COMPRESSIVE CUEING RECEIVER

Analysis Bandwidth	3.0 GHz (7.0-10.0 GHz)
Frequency Resolution	110 MHz
Frequency Bins	28
Analysis Time	128 ns
Maximum Cryogenic Temperature	83 K
Cryogenic Power Consumption	5 mW (cables), plus radiative heat load
Total Ambient Power Consumption	20 W (not including cryocooler power)



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Fig. 10. Illustration of wafer bonding and thinning technique used to fabricate 40-ns YBCO chirp filters on 125- μ m-thick, 2-in-diameter LaAlO_3 substrates. The chirp filters are constructed in a stripline structure. A photograph of a Hamming-weighted 40-ns filter is shown as an inset. The impedance transformers are based on a Klopffenstein taper [48].

the microwave transitions in and out of the filter. The YBCO film stops short of the edge of the LaAlO_3 wafer, requiring long bond wires and a nonstandard launcher configuration for the initial 24- and 40-ns chirp filters. As shown in an inset to Fig. 10, these saw-cut notches allow a more reasonable microwave transition to be made, greatly reducing bond-wire length. The gold plating shortens the ground-plane contact path and therefore reduces inductance at the transition. Further enhancements along these lines are possible.

The improved 40-ns YBCO chirp filter produced -18 -dB error sidelobes, once again the limit of the modified HTSSE SLO. Fig. 11(b) shows this compressed-pulse performance for the combination of the SLO and the improved 40-ns chirp filter. The measurement is made by the repetitive sampling of a

digital oscilloscope to capture the compressed-pulse envelope.

The bonded/thinned-wafer technique used to produce 5-mil-thick substrates on 2-in-diameter LaAlO_3 wafers will scale directly to 3-in diameter LaAlO_3 wafers, enabling dispersive delays of 90 ns, or to 4-in-diameter LaAlO_3 wafers, enabling delays of 160 ns. In both cases, thinner bonded substrates would produce longer delays. For these longer chirp filters, YBCO ground planes will be required to limit dissipation loss. This is in place of the gold ground plane shown in Fig. 10.

VI. DEMONSTRATIONS WITH EXISTING COMPRESSIVE-RECEIVER HARDWARE

Demonstrations have also been performed with existing compressive-receiver hardware to produce complete signal

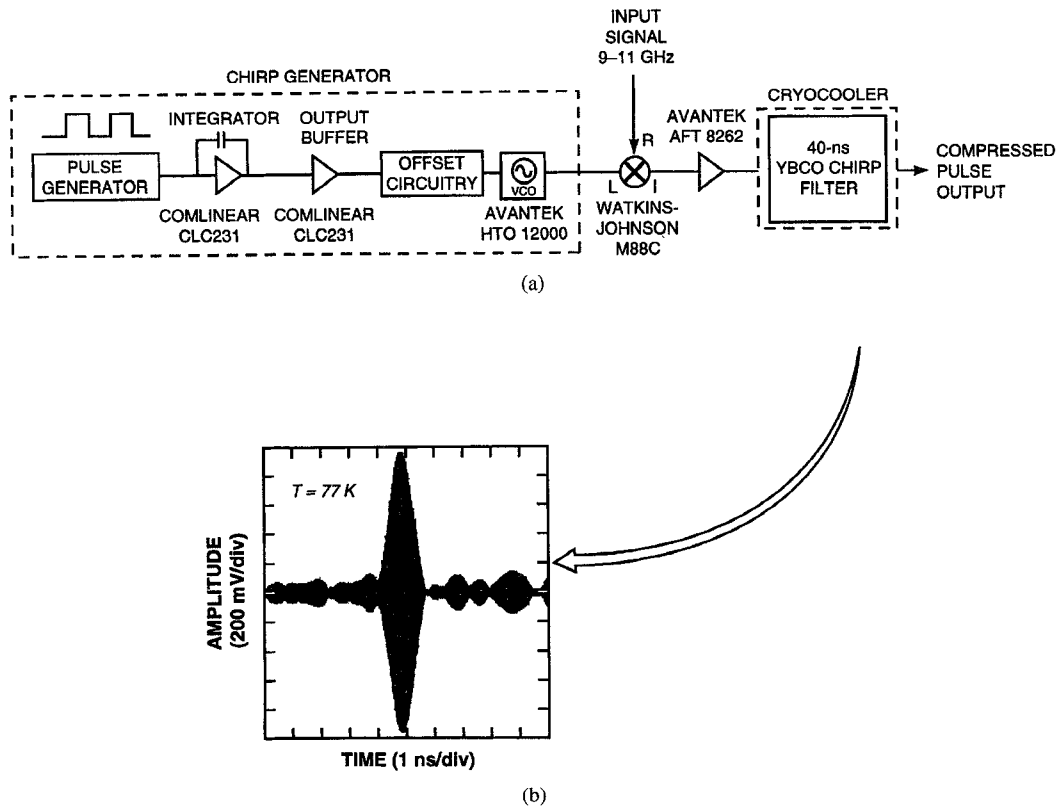


Fig. 11. (a) Detailed schematic diagram of compressed pulse test setup. The chirp generator is used to generate an upchirp waveform, which is then compressed into a pulse using the downchirp ports of the 40-ns YBCO chirp filter. (b) Compressed-pulse envelope measured at 77 K for the test setup combination of chirp generator and improved 40-ns YBCO chirp filter. This setup produced SLO-limited error sidelobe levels of -18 dB.

reports as is done in a stand-alone EW receiver [46]. A complete demonstration was recently performed with Hughes Aircraft Company, replacing the Hughes receiver's 1-GHz 200-ns SAW chirp filters with a 2-GHz 24-ns HTS YBCO chirp filter and VCO-based SLO. Although the analog and digital electronics in the Hughes receiver is matched to the narrower bandwidth of the SAW filters, the receiver was demonstrated to have full functionality with 2-GHz bandwidth HTS chirp filters at the front end. This demonstration doubled the instantaneous bandwidth coverage of the receiver. In order to produce a meaningful demonstration, an HTS chirp filter with at least 24 ns of dispersive delay was required to fill a significant portion of the 200-ns receiver analysis window.

The Hughes compressive receiver is a completely self-contained EW receiver, capable of producing pulse descriptor words on multiple emitters. The descriptor words describe the emitter frequency, amplitude, pulse width, pulse repetition interval, and time of arrival (TOA). The input frequency range for the demonstration was 9.8–11.8 GHz. A ramp generator and VCO combination functioned as a chirp generator to produce an upchirp, again using the M(l)–C(s) chirp-transform algorithm. The results of the Lincoln/Hughes demonstration are listed in Table IV. The frequency-versus-time characteristic of the HTS chirp filter is significantly better than the characteristic of the VCO-based chirp generator, as described in the last section. The error sidelobe levels set by the chirp generator act as spurious signals, limiting the single-tone dynamic range to 30 dB for a given signal detection threshold. A 50-

dB dynamic range was obtained by adjusting the detection threshold. The receiver is limited to 200-ns TOA resolution and only 50% probability of intercept for short (100–400 ns) pulses because the receiver was designed to operate with 200-ns-long SAW chirp filters and a 200-ns analysis window. The frequency resolution of 83 MHz is somewhat limited since the receiver's 1-GHz log amplifiers elongate the 2-GHz-bandwidth compressed pulses generated by the HTS chirp filters. No more than three simultaneous signals can be detected because the detected compressed pulses must be at least 10 ns apart, and the HTS chirp filter is only 24 ns long.

Some preliminary demonstrations have also been done using linearized VCO-based SLO technology developed by AIL Systems [49], [50]. These demonstrations have resulted in reasonable performance from a combination of a linearized SLO and an initial 24-ns YBCO chirp filter [51]. Future efforts should result in an excellent combined performance, eliminating the SLO limitations described here.

VII. NOVEL WIDEBAND HTS COMPRESSIVE CRYORECEIVER

Fig. 12 outlines a novel compressive cryoreceiver architecture. There are several key features to this new architecture, particularly the use of digital technology to perform pulse detection and preprocessing. This does not rule out the hybrid use of more traditional analog pulse detection [8], but allows receiver performance to be significantly improved. The cryoreceiver aspects of the architecture are generic to other types of microwave receivers.

TABLE IV
SUMMARY OF LINCOLN/HUGHES JOINT COMPRESSIVE RECEIVER DEMONSTRATION¹ (TAKEN FROM REFERENCE [46])

Parameter	Measured Performance
RF Input Bandwidth	2.0 GHz
RF Frequency Resolution	2 GHz/24 cells = 83 MHz
Time of Arrival and Pulse Width Resolution	200 ns
Dynamic Range, Single Tone	30 dB*
Simultaneous Signal Detection	Up to 3
Short-Pulse (100-400 ns) Probability of Intercept	50%
Long-Pulse (>400 ns) Probability of Intercept	100%
Amplitude Resolution	1 dB
* >50 dB with manual threshold adjustment.	

Fig. 12(a) illustrates the overall receiver and makes clear the potential to use additional cryoelectronic components to enhance performance. The overall receiver is a three-channel compressive receiver, using a monopulse antenna to determine angle of arrival by measuring monopulse-channel signal amplitudes only. Relative phase extraction for interferometry could also be performed but would require an additional digital channel for each analog channel [20]. The configuration is an M(l)-C(s), and the signal reports are used to cue narrowband receiver assets for signal demodulation. These signal reports also represent a complete parameterization of frequency, amplitude, pulse width, time of arrival, and angle of arrival. The HTS delay line provides the local oscillator (LO) controller time to reconfigure. Since HTS analog delay lines are expected to be no longer than about 200 ns, this would stress the speed of the LO controller. However, fast-tuned oscillator technology has been demonstrated with 100-ns tuning times for smaller bandwidths [52].

Although the HTS chirp filters enable the wideband compressive receiver, additional cryoelectronic components can significantly enhance receiver sensitivity and dynamic range. Initial demonstrations or investigations of many of these components have already been made. Cryocooled low-noise amplifiers [53], [54] and mixers [55], [56] will improve sensitivity by lowering the noise figure of the amplifier and reducing the conversion loss of the mixer. Adaptive notch filters [57] and tunable preselect filters [58], [59] will improve dynamic range by eliminating spurious signals or out-of-band noise. Any downconversion process is performed at cryogenic temperature [60] in conjunction with the SLO mixing with the input signals. An HTS delay line provides low loss and corresponding low noise figure to enhance the sensitivity of the superheterodyne receivers [25], [61].

The advanced semiconductor pulse processing circuits shown in Fig. 12(b) move the analog-to-digital (A/D) interface as close to the analog chirp-transform process as possible. An envelope detector strips the rf carrier from the compressed pulse, reducing the effective bandwidth of the pulse from that of the carrier to that of the compressed-pulse envelope. This greatly reduces the required analog bandwidth of the log amplifier and the sample rate of the A/D converter. The envelope detector and log amplifier precede a high-

speed 6-bit 3-GS/s GaAs heterojunction bipolar transistor (HBT) A/D converter [62] to provide a single-signal 60-dB dynamic range for a 4.0-GHz-bandwidth HTS compressive receiver. A demultiplexer circuit [63] reduces the clock rate requirement for the data-thinning application-specific integrated circuit (ASIC). The best choice for the ASIC is silicon-on-insulator (SOI) CMOS which is both high-speed and low-power [64]–[66]. Binary integration over multiple analysis windows is performed on the appropriate binary level to enhance the sensitivity [67], [68]. The data-thinning process is key so that the digital signal processing (DSP) board is not overloaded. The thinned pulse-detection data is passed on to a DSP board for frequency and amplitude accuracy enhancement through interpolation techniques using knowledge of the pulse envelope shape and a number of digital samples to determine the actual pulse centroid. These techniques should conservatively improve frequency accuracy, for example, by a factor of four. The techniques can also be used to identify the amount of partial window filling at the leading and trailing edges of a pulse to enhance pulse width or TOA accuracy. This is in sharp contrast to the difficulty partial filling of the analysis window creates for analog pulse detection techniques, substantially degrading pulse-width accuracy to the length of an analysis window [8].

The use of binary integration to enhance sensitivity was previously demonstrated as part of a packet radio [67], [68]. In that communication application the phase of the carrier was known and the integrations were done coherently. In this case the integrations are noncoherent. A coherent integration process will always yield an N improvement in sensitivity while a noncoherent process asymptotically approaches a $4(N)^{1/2}$ improvement for a large number of integrations. However, for small numbers of integrations the difference between coherent and noncoherent can be quite small [69]. This difference is somewhat a function of the false alarm rate and probability of detection, i.e., the required minimum signal-to-noise ratio. For 100 integrations a coherent process will yield a 20-dB improvement, a noncoherent process will yield approximately 15 dB (not 10 dB as an oversimplified $N^{1/2}$ calculation would predict). As a further example, compare the use of binary integration, first with only a 40-ns HTS chirp filter and then with both a 500-ns SAW chirp filter and a 40-ns HTS chirp filter. Recall that the sensitivity is independent of bandwidth, and that pulse compression is a

¹ Performed with a 24-ns, 2-GHz-bandwidth YBCO chirp filter.

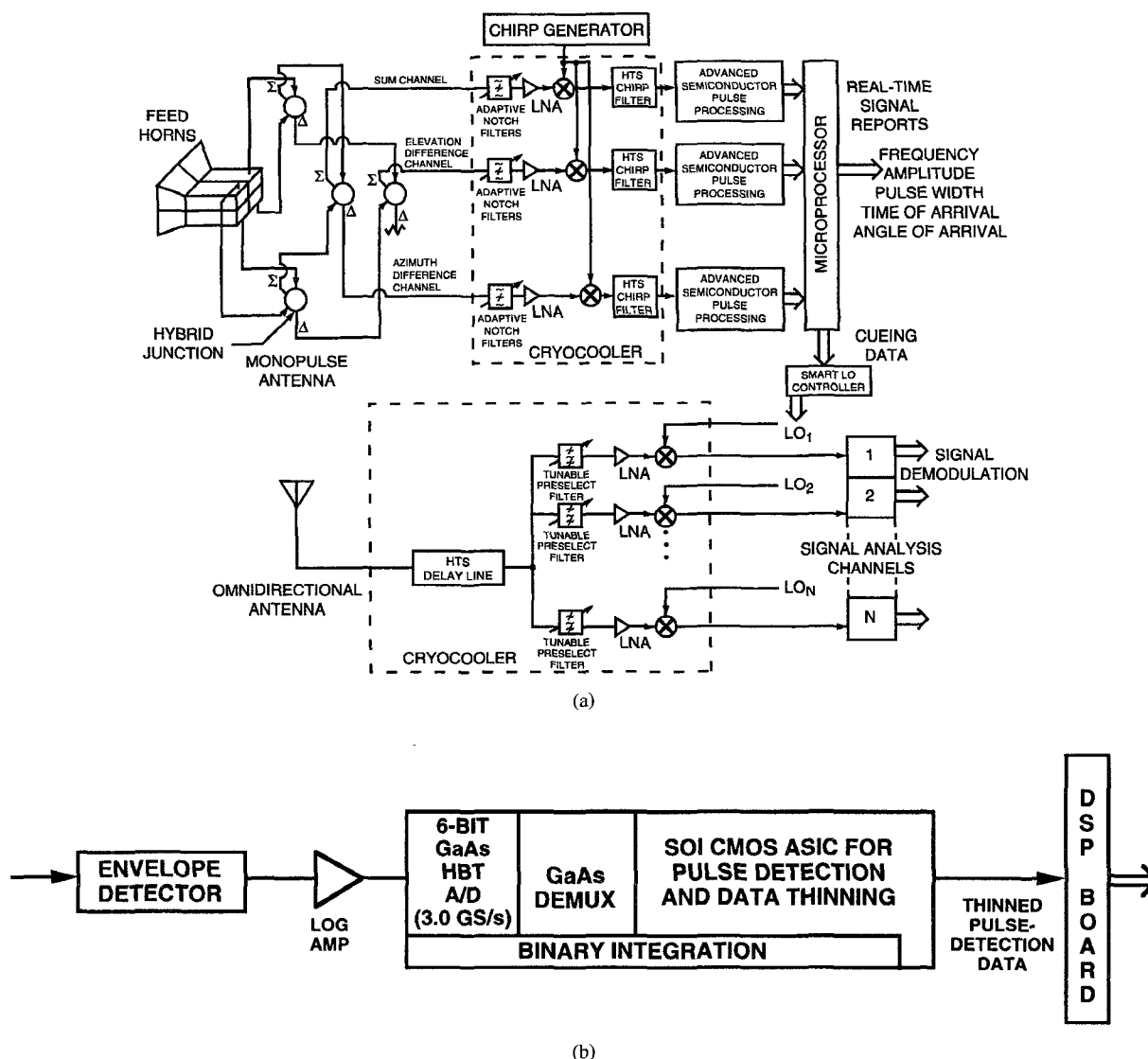


Fig. 12. (a) Concept for compressive cryoreceiver, including cued narrowband cryoreceivers for signal demodulation. The compressive cryoreceiver core will produce real-time signal reports of frequency, amplitude, pulse width, time of arrival, and angle of arrival. These reports will then be used to cue the narrowband cryoreceivers. (b) Detailed schematic of proposed advanced semiconductor pulse processing electronics of the compressive cryoreceiver.

coherent (analog) process equivalent to an integration. The 500-ns SAW filter is 12.5 times longer than the HTS filter, but the HTS filter can have 12.5 noncoherent binary integrations performed in that time. The SAW filter alone will have only 2 dB more sensitivity than the HTS filter with a noncoherent integration process because a small number of integrations is involved. The binary integration process can also be invoked for each 500-ns frame of the SAW device. In the limit of a large number of integrations, the SAW device will always perform 12.5 times fewer noncoherent integrations than the HTS device, giving it a maximum sensitivity advantage of $5 \log(12.5) = 5.5$ dB over the HTS device. But recall that the other cryoelectronic components in the HTS receiver will enhance sensitivity, particularly at higher frequencies, in a way unavailable to a SAW system. This additional enhancement could equal or exceed the maximum 5.5 dB difference, while maintaining the short-pulse capability of the shorter HTS lines by avoiding partial filling of the analysis window for short pulses.

To establish a baseline for the amount of digital signal processing required, consider that only one set of DSP operations per pulse might be needed to enhance frequency accuracy. The processor would then keep track of that emitter on a coarser scale. Assuming a very generic 1-Mpulse/s signal environment and assuming a conservative 25 operations to determine the pulse centroid, a processing rate of only 25 MFlops is required. This is 10^4 times less than the operations required to implement an all-digital receiver. At this level, the DSP circuitry requires only a small fraction of the receiver size, weight, and power. Enhancement of TOA through DSP operations to identify the amount of partial analysis-window filling at the leading and trailing pulse edges would require an additional 50 operations per pulse producing a total requirement of 75 MFlops.

Some size, weight, and power estimates can be made by taking into account the need for a cryocooler and its control electronics. A typical cryocooler/controller combination (Stirling cycle) will require 25–50 W, 0.5–2.0 kg, and

TABLE V
DIGITAL SIGNAL PROCESSING EQUIVALENT (FLOPS) FOR VARIOUS COMPRESSIVE RECEIVERS

		BW (GHz)	N	Duration NT (ns)	Frequency Resolution (MHz)	Equivalent DSP Rate (GFlops)
HTS Compressive	{	10.0	2048	102.4	9.8	1320
		3.0	512	85.4	12	324
		3.0	256	42.7	23	288
		3.0	128	21.3	47	252
SAW Compressive	{	1.0	256	128	7.8	96
		0.30	8192	13660	0.073	47
		0.30	128	213	4.7	25
		0.050	4096	40960	0.024	7.2

0.1–0.2 ft³ for 0.5–1.5 W of cooling power near 70 K. The receiver system described, making use of new semiconductor monolithic components, translates into a small number of ASIC chips per channel, possibly on a single board. This receiver solution can readily be estimated to consume well under 200 W for a three-channel compressive receiver. The receiver architecture is also better suited to handle much wider bandwidths than a receiver approach based on multiple analog pulse-detection and processing boards. Timing uncertainties between boards would preclude their use for bandwidths of 20 GHz where timing accuracies of <10–20 ps would be the norm.

The proposed HTS compressive cryoreceiver architecture is capable of unprecedented multigigahertz bandwidth coverage per channel, translating into a small size, weight, and power receiver. Compared to SAW receivers the HTS receiver could have the same or better sensitivity, similar frequency accuracy and resolution, the same or better amplitude accuracy, greatly improved TOA and pulse-width accuracy, improved dynamic range, and greatly improved short-pulse capability.

VIII. COMPARISON TO CONVENTIONAL TECHNOLOGY

A. Comparison to All-Digital Receiver

The signal-processing power of an analog Fourier-transform process becomes evident with a comparison to the equivalent digital fast-Fourier-transform (FFT) process in floating-point operations per second (Flops) to achieve the same frequency accuracy and resolution. Recall that an N -point FFT has a frequency resolution of $1/NT$ Hz where T is the sampling interval [70]. The maximum frequency that can be sampled and satisfy the Nyquist criterion is $f_{\max} = 1/2T$ Hz. As long as the signal of interest can be brought down to baseband, f_{\max} is equal to the receiver analysis bandwidth B_R . In order to perform an FFT in real time, the FFT must be completed during the duration of the signal, which is equal to NT . Assuming N is a power of two, $(N/2) \log_2 N$ butterflies are required for an N -point FFT. The modern SHARC DSP chip (Analog Devices ADSP-2106X) performs an N -point complex FFT in $2N \log_2 N$ clock cycles with 3 Flops/cycle (120 MFlops on 40-MHz clock) [71], resulting in the following

DSP rate to perform an N -point complex FFT:

$$\begin{aligned} \text{DSP Rate (Flops)} &= \frac{19.92}{NT} N \log_{10} N \\ &= 2f_{\max} (19.92) \log_{10} N. \end{aligned} \quad (7)$$

Table V lists examples of the digital equivalents in Flops to analog chirp-transform algorithms relevant to HTS and SAW compressive receivers.

It is also important to recognize that round-off “noise” will require extra bits to be carried internally to support the desired dynamic range in the DSP FFT [72]. For an N -point FFT using internally scaled fixed-point arithmetic the power ratio of round-off “noise” to ideal output is $4N2^{-2b}$ where b is the number of bits carried in the computation. Fixed-point DSP chips usually clock slightly faster than their floating-point counterparts. A dynamic range of 2% requires $b = b_0 + (1/2) \log_2 4N$ where $(1/2) \log_2 4N$ is the number of extra bits needed internally. For example, for a 60-dB dynamic range in a 1024-point FFT, 16 bits are required internally to provide 10 bits at the output.

The success of VLSI/ULSI CMOS and BiCMOS circuits has led to dedicated fixed- and floating-point DSP chips. As an example, the MeshSP-1 synchronous processor [71] is an 8×8 array of sixty-four SHARC DSP chips and is capable of 7.7 GFlops throughput requiring approximately 100 W for two 7.25×13 -in circuit boards. This is approximately the equivalent of a 50-MHz-bandwidth 40- μ s-long analog chirp-transform algorithm in a SAW compressive receiver. Scaling directly by a factor of 40 to 300 GFlops would require a minimum 4 kW of power (and require over 2500 DSP chips), clearly not a small size, weight, and power solution and more than ten times the estimate for the HTS compressive receiver.

B. Comparison to Channelized-Filter Receiver Architectures

A comparison to channelized-filter architectures can also be made by determining the minimum number of filters required in a bank of filters to achieve the same frequency accuracy as the novel HTS compressive-receiver architecture described in the last section. Table VI lists examples of this comparison for 3- and 10-GHz-bandwidth receivers. If the comparison focuses on the core function of the receiver and assumes that

TABLE VI
PROJECTIONS FOR FREQUENCY ACCURACY OF WIDEBAND COMPRESSIVE RECEIVER WITH 100-ns HTS CHIRP FILTER

	Frequency Accuracy	Minimum No. Filters	Equivalent No. Channelizing Filters†
HTS Compressive Receiver (3-GHz BW)			
Without interpolation	13.3 MHz	1	225
With conservative interpolation	3.3 MHz	1	900

HTS Compressive Receiver (10-GHz BW)			
Without interpolation	13.3 MHz	1	750
With conservative interpolation	3.3 MHz	1	3000

†Assumes channelizing-filter architecture does not use interpolation.

the signal-report electronics is either separate or consumes a negligible fraction of the receiver, then a compressive receiver consisting of a single HTS chirp filter in a cryostat and several ASIC chips for pulse detection (and signal report) could reasonably consume ten times less size and weight than 3000 rf filters. Interpolation techniques would reduce the required number of filters at the expense of added complexity.

The channelized-filter approach must also contend with the transient (or rabbit-ear) phenomenon in which the $\sin x/x$ sidelobe components of a received rf pulse spread out into adjacent filter channels [8]. This is a particularly difficult problem for short rf pulses. The compressive receiver, in contrast, divides each received pulse into smaller analysis windows that are weighted (Hamming is a good example) to produce small, well-behaved sidelobes. There is no way to introduce such an apodization scheme into a channelized-filter approach without adding greatly to the receiver complexity. Gaussian weighting each of the channelized filters will help somewhat, but the channelized-filter bank must contend with the frequency sidelobes produced by the input signal. This has led to the practice of using two filters in cascade for each channel, the first a narrower bandwidth but with few poles and the second a wider bandwidth and with many poles. This of course adds to the size and weight of channelized-filter receivers. The transient phenomenon also makes the use of interpolation more difficult.

This transient phenomena often forces the use of wider bandwidth channels than desired in a channelized-filter architecture, thereby degrading sensitivity. It is not unusual to find that a compressive receiver can be configured with 5–10 dB better sensitivity than a channelized-filter receiver [6]. For comparison purposes, the sensitivity of a compressive receiver can be calculated using (1) the noise over the entire bandwidth B_R of the receiver along with the TB_c signal processing gain, or (2) the noise over the frequency resolution bandwidth $\Delta f = k/T$ without the signal processing gain. These two methods are equivalent and point to the excellent sensitivities that can be obtained with compressive receivers. However, the channelized-filter approach does presently offer an advantage in two-signal spurious-free dynamic range over an HTS wideband compressive receiver. This could outweigh any sensitivity advantage depending upon the application.

IX. FUTURE DEVELOPMENTS

There are no physical limitations to prevent near-term advances in both HTS chirp-filter technology and the advanced semiconductor circuits described previously. The HTS chirp filter is based on electromagnetic delay lines. The low measured losses in HTS thin films and careful rf design should allow the bandwidths of HTS chirp filters to reach 20 GHz. Cryocooler efficiency, reliability, size, and weight will continue to improve, driven by infrared and HTS technologies. Transition temperatures of HTS materials may improve somewhat as well. Cryocooled semiconductor digital components and even HTS digital components [73] are much longer term possibilities.

It is not difficult to project the near-term future of the advanced semiconductor circuits described in Section VII. Moore's Law and variations thereof tell us that circuit densities and speeds in VLSI/ULSI CMOS have doubled roughly every 18–24 months, and that trend will continue for some time to come until a physical/economic limit is reached [74]. A 6-bit 3.0-GS/s A/D will eventually be replaced by a 6-bit 10-GS/s A/D, and so on. The capability of the DSP chips will improve as measured in both clock speed and operations per second. It is entirely feasible that the capabilities of SAW compressive receivers will be surpassed in the next ten years by all-digital receivers consuming less than 100 W. In contrast, the equivalent digital signal processing capability of HTS compressive receivers will approach 3 TFlops over the same time frame in a much smaller size, weight, and power package than would be possible with digital technology alone.

X. CONCLUSION

HTS chirp filters have reached the level of maturity to represent an enabling technology for compressive receivers with bandwidths greater than 1 GHz. This is the widest instantaneous analysis bandwidth per channel for any receiver technology, and translates into a receiver having very small size, weight, and power requirements.

Dispersive delay in HTS chirp filters has been increased to 40 ns by using a bonded/thinned-wafer technique, giving time-bandwidth products in excess of 100. Chirp filters with multigigahertz bandwidths have been demonstrated in YBCO

stripline structures with 24-ns dispersive delay on 10-mil-thick, 2-in-diameter bonded-wafer LaAlO_3 , and with 40-ns dispersive delay on 5-mil-thick, 2-in-diameter bonded/thinned-wafer LaAlO_3 . Both 24- and 40-ns filters have produced better than -18 -dB error sidelobes. Chirp filters had previously been demonstrated with 8 and 12 ns of dispersive delay in YBCO on self-supporting 20-mil-thick, 2-in-diameter LaAlO_3 .

Several compressive receivers have been reported here that function at bandwidths unavailable with conventional chirp-filter technology. A space-qualified HTS compressive cueing receiver was designed and built for flight in the Navy's HTSSE space experiment on the Air Force ARGOS scientific satellite. The 3.0-GHz instantaneous analysis bandwidth demonstrated in the prototype and space-qualified HTSSE compressive cueing receivers was unprecedented. This HTSSE cueing receiver provided a frequency resolution of 110 MHz with a 19-dB dynamic range over a 7.0–10.0-GHz input band. In addition, an existing Hughes compressive receiver, operated as an HTS compressive receiver, demonstrated a frequency resolution of 83 MHz with a 50-dB dynamic range across a 2.0-GHz band from 9.8–11.8 GHz. This modified receiver detected up to three simultaneous emitters with a 1-dB amplitude resolution and 100% probability of intercept for pulses greater than 400 ns.

A novel compressive cryoreceiver architecture has been proposed here combining HTS, cryoelectronic, and advanced high-speed semiconductor technologies. This compressive receiver architecture will readily rival the sensitivity of a narrowband receiver while providing instantaneous frequency coverage over up to a 4-GHz band using a 3.0-GS/s A/D immediately following the analog chirp-transform subsystem. The high-speed serial nature of the compressive receiver output is well matched to emerging semiconductor components. Future technology developments are poised to extend this bandwidth capability. The widest-bandwidth real-time simultaneous-signal analysis capability, the reduced size, weight, and power, and the opportunity for insertion of additional HTS and cryoelectronic components to enhance receiver sensitivity and dynamic range, make the wideband compressive receiver a very attractive application niche for analog HTS microwave filters. Relatively short 40-ns HTS chirp filters produce very good short-pulse analysis capability, but not at the expense of other receiver parameters. In fact, the novel features of the proposed receiver will improve many parameters over SAW compressive receivers.

Requirements exist for this receiver in electronic warfare and remote sensing. Detailed comparisons of the HTS wideband compressive receiver (including cryocooler) to an all-digital receiver and to channelized-filter receiver architectures have identified the compressive receiver as superior to the others by better than one order of magnitude in size, weight, and power. Several important advantages of HTS compressive receivers over acousto-optic channelizers have also been noted, especially the wider bandwidth coverage per receiver channel.

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well as rf circuits and systems for communication, radar, remote sensing, and instrumentation, which involves systems in both the commercial and military sectors.

Dr. Lyons is listed by *American Men and Women of Science*, and is a member of Sigma Xi, Eta Kappa Nu, Tau Beta Pi, the Association of Old Crows, and the American Physical Society.



Duane R. Arsenault was born in Gardner, MA, on November 28, 1952. He received the BSEE degree from Worcester Polytechnic Institute, Worcester, MA, in 1974, and the Master and Doctor of Engineering degrees in electrical engineering from Rensselaer Polytechnic Institute, Troy, NY, in 1975 and 1979, respectively.

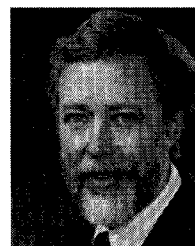
Since November 1978, he has been a member of the technical staff, Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, where he has been involved in the development of signal processing, radar, and communication devices and technology. His earlier work involved the development of systems incorporating SAW chirp filters. These include a digitally interfaced Fourier-transform processor, a multiple-channel spectrum analyzer and narrowband excision in a wideband SAW-convolver-based spread-spectrum packet-radio communication receiver for which he also developed an error-control subsystem. His papers contributed during this time period describe the practical implementation of the chirp-transform techniques employed in these particular applications. More recently, he has been involved in the development of high-performance CMOS/CCD programmable binary correlators intended principally for upgrade of NASA's advanced tracking and data-relay satellite system (TDRSS), for which a dual 256-tap CCD correlator was successfully produced. His most recent work involves the development of low-power CCD correlators and signal processing devices, and wideband compressive receivers incorporating superconducting chirp filters.

Alfredo C. Anderson, photograph and biography not available at the time of publication.



W. Gregory Lyons (S'81-M'88) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Illinois, Urbana, in 1982, 1983, and 1989, respectively. His M.S. degree work involved the development of optoelectronic and microwave devices, particularly HEMT's and HBT's, based on GaAs and related III-V semiconductors. His Ph.D. work was a study of collective quantum-mechanical effects in low-dimensional metallic conductors, including a critical examination of potential macroscopic quantum phenomena at temperatures near ambient.

Since March 1989, he has been a staff member in the Analog Device Technology Group, Lincoln Laboratory, Massachusetts Institute of Technology, Lexington. His work there includes the development, design, and fabrication of superconducting microwave devices and their implementation in high-performance signal-processing systems. This work has been focused mainly on using thin-film high-T_c superconductors to build and demonstrate passive analog microwave devices such as narrowband filters, resonators, delay lines, chirp filters, and antenna feed networks. He has worked within the Consortium for Superconducting Electronics since its inception in 1989. He was responsible for a joint Lincoln/COMSAT/AT&T delivery of a space-qualified narrowband filter for the Navy's first HTS space experiment (HTSSE I), in addition to his contribution in Lincoln's delivery of an HTS compressive receiver for the Navy's second space experiment (HTSSE II). His present research interests include the fundamental properties of superconductors, as



T. C. L. Gerhard Sollner (M'78-SM'91) received the Ph.D. degree in physics from the University of Colorado, Boulder, in 1974, with a thesis on magnetic interactions in insulators.

He contributed to observational submillimeter astrophysics at the University of London, Queen Mary College, for the next two years. From 1976 to 1980, he helped develop millimeter-wave astronomical receivers, especially an 80-90 GHz maser at the Five College Astronomy Observatory, University of Massachusetts, Amherst. He joined the faculty, Department of Electrical Engineering, University of Massachusetts, in 1980, continuing work on superconductor-insulator-superconductor junctions for sensitive astronomical receivers. In 1982, he became a Staff Member, Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, where he is now the Leader of the Analog Device Technology Group. At Lincoln Laboratory, he has been instrumental in showing that resonant tunneling could be useful for devices into the terahertz region, and the development of several novel devices based on that fact. His current research interests include signal-processing applications for superconductive and resonant-tunneling devices. He holds three patents and has published more than 30 refereed papers.

Dr. Sollner is a member of the American Physical Society and the Association of Old Crows.



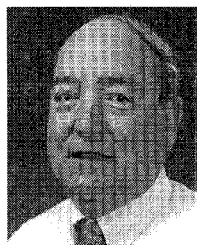
Peter G. Murphy was born in Cambridge, MA, in 1949. He received the B.S. degree in marine biology from Southampton College, Southampton, NY, in 1975, and the B.S. degree in electrical engineering technology from the Wentworth Institute of Technology, Boston, MA, in 1987.

He has been with the Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, since 1984, involved in fabrication process development and thin-film research as applied to superconductive analog devices.



Mark M. Seaver received the B.S. degree from Lowell University, Lowell, MA, in 1989.

He joined the Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, in 1981, and has been an Assistant Staff Member since 1990. His research interests are in designing, building, and testing high-speed circuits that are used in silicon CCD signal-processing devices and in system applications of high- T_c superconductive analog devices.

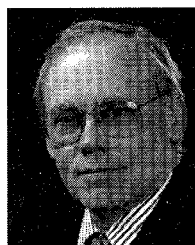


Rene R. Boisvert was born in Fitchburg, MA, in 1942. He graduated from technical school and from the U.S. Navy electronic school (class A, class C). He was an electronic fire-control technician in the Navy from 1962 to 1966.

He joined the Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, in 1966. In 1977, he joined the Analog Device Technology Group, Lincoln Laboratory, where his work has involved the development of architectures and circuits for the demonstration and application of advanced

analog signal-processing devices.

Richard L. Slattery attended Tufts University, Medford, MA, from 1965 to 1969 as a chemistry major, and began working for the Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, in 1969. He was involved in early efforts to fabricate surface-acoustic-wave devices using electron-beam lithography. He worked for an acoustic engineering firm from 1970 to 1973, and returned to Lincoln in 1974. Since 1978, he has been on the staff of the Analog Device Technology Group, involved with the fabrication and packaging of acousto-electric and superconducting devices.



Richard W. Ralston (S'62-M'65-SM'94) received the B.S. (with highest honors) and the M.S. degrees in electrical engineering from Lehigh University, Bethlehem, PA, in 1964 and 1965, respectively, and the Ph.D. degree in applied physics from Yale University, New Haven, CT, in 1971.

From 1965 to 1966, he was a member of the technical staff, Bell Laboratories, where he participated in the development of solid-state microwave sources. He joined the Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, in 1971, to develop tunable diode lasers in the Applied Physics Group. In 1974, he moved to the Analog Device Technology Group, which he led from 1984 to 1995. The group's principal efforts have been the development of surface-acoustic-wave filters, charge-coupled devices, and superconductive components, with a unifying mission of creating power-efficient electronic subsystems for high-throughput, real-time signal processing. He is currently associate head of the Solid State Division, Lincoln Laboratory, overseeing a broad range of research directed at extending the performance of advanced optoelectronic devices and electronic circuits with a goal of enabling new system applications. He also has served as principal director of the Consortium for Superconducting Electronics (CSE) since its creation in 1989. He holds several patents and has authored more than 50 published technical papers.

Dr. Ralston is a member of Phi Beta Kappa, Tau Beta Pi, and Eta Kappa Nu.